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MESSAGE: **NOTICE OF APPEAL FROM THE EXAMINER TO THE BOARD OF PATENT APPEALS AND INTERFERENCES and PRE-APPEAL BRIEF REQUEST FOR REVIEW**

Patent Application No. 09/449,912
Applicant: Divittorio
Filed: December 2, 1999
TC/AU: 2195
Examiner: Kenneth Tang
Docket No.: 202232 (Client Reference No. 99,032)
Customer No.: 23460

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

Applicant requests review of the final rejection, dated December 12, 2005, in the above-identified application. No amendments are being filed with this request. This request is being filed with a notice of appeal. An appeal brief has not yet been filed. This Pre-Appeal Brief Request For Review is submitted for the reason(s) stated on the attached sheets. An appendix containing the set of presently pending claims is attached for your convenience.

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Name (Print/Type)	Jacquelyn Hurd		
Signature	Jacquelyn Hurd	*Date*	June 12, 2006

Applicant traverses the final rejection of the pending claims. In an effort to minimize the issues addressed during this review, Applicant has focused primarily upon claim 1, also requests consideration of the other rejected claims as well, including certain dependent claims for which the Final Office Action does not identify at least one recited element in the prior art. Applicant requests pre-appeal brief review of the final rejection of because the final rejection does not show proper motivation to modify Applicant's admitted prior art in a manner that would combine the two recited functionalities into a control processor as recited in claim 1. Nowhere do the cited references disclose or suggest the presently claimed process controller and method wherein an embedded application program that calculates set point values for the control processor is executed on the process controller at a lower assigned priority than a set of control blocks. For at least this reason, the presently pending claims are in proper form and patentable over the prior art presently known to Applicant.

Applicant's Representative Pending Claim 1

1. A control processor for executing a set of control tasks defining dynamic model-based interactive control of an industrial process, the control processor comprising:

an embedded control task-comprising a multivariable linear program including a set of output values corresponding to process setpoints; and

a set of control blocks including regulatory control blocks having output values that are transmitted by the control processor to field devices coupled to the industrial process, wherein the embedded control task executes at a lower execution priority than an execution priority of the set of control blocks.

Reasons for Pre-Appeal Brief Request For Review

Applicant traverses the rejection of the pending claims for all the reasons set forth in the previous response submitted on September 20, 2005, and incorporates the remarks at pages 10-13 therein. The Final Office Action presents the same grounds as provided in the previous Office Action and therefore contains the same errors addressed in Applicant's previous response. The most significant error is the complete absence of any teaching of motivation in the prior art to incorporate the embedded control task into a control processor, and execute the embedded control task at a lower priority than the set of control blocks. In

addition to Applicant's previous remarks incorporated herein by reference, Applicant addresses the Final Office Action's comments regarding Applicant's previous remarks.

1. Addressing the Final Office Action's statement in **section 19** regarding the proper interpretation of claims, Applicant recognizes the responsibility of the USPTO, during prosecution of an application, to give claims within the application a broadest *reasonable* interpretation. However, Applicant's object to an interpretation, by the Final Office Action, of the pending claims that contradicts the meaning of claim elements that have been defined by Applicant's disclosed embodiments and further explained in Applicant's responsive remarks – that also cannot be disregarded in a reasonable interpretation of the claims. See, *Phillips v. AWH Corp.*, 75 USPQ2d 1321 (Fed. Cir. 2005). As evidenced by the USPTO's participation in the briefing of the *Phillips* Appeal, this recent decision of the Federal Circuit applies to both application prosecution and patent litigation contexts. As explained in *Phillips*, claims must be reasonably interpreted in view of the specification, which is highly relevant to claim construction analysis, and is the single best guide to determining the meaning of terms. The meaning of a claim is furthermore interpreted in view of an Applicant's remarks in attempting to explain and obtain a patent. Thus, the Final Office Action cannot justify a failure to recite teachings of claim elements in the prior art by interpreting the claim elements in a way that is contrary to the disclosure and Applicant's remarks explaining the scope of the claimed invention.

2. The Final Office Action does not present a *prima facie* case of obviousness.

Applicant submits that the final rejection does not show proper motivation to modify Applicant's admitted prior art (AAPA) in a manner supporting the obviousness rejection of claim 1. In particular, Applicant submits that Iino does not disclose or provide motivation to one skilled in the art to provide a control processor that includes both (1) an embedded control task and (2) a set of control blocks including regulatory control blocks having output values for field devices coupled to an industrial process, and wherein the embedded control task operates at a lower execution priority than the set of control blocks. As Applicant previously explained at page 10 in the preceding response, Iino discloses two separate and distinct hardware devices (predictive control apparatus 1 and process control unit 30) for providing the functionality recited in claim 1. Since the two functions are carried out on different hardware, there is no need to even consider carrying out the functions at two different levels of priority. Applicant addresses the Final Office Action's obviousness

rejection of claim 1 further in item "4" (addressing **section 22** of the Final Office Action) below.

Addressing the argument in **section 20** of the Final Office Action, Iino explicitly discloses *executing the two recited computing functions in two separate hardware devices.* The Final Office Action states that "the motivation would be to optimize performance based on changing multiple variables or minimize cost." However, Iino does not even disclose combining the two recited functions into a single control processor. Furthermore, the Final Office Action, at **section 20** does not explain its assertion that combining the functions recited in claim 1 optimizes performance or minimizes cost. With regard to "optimizing performance," combining the two functions in a single control processor increases the probability that the control processor will not be able to complete all of its scheduled activities in a single cycle – which would appear to reduce performance. With regard to "cost savings," the claimed invention does not necessarily eliminate the costs associated with hardware executing at a supervisory level. For example, workstations that are capable of executing the embedded control task still reside on a supervisory process control network to facilitate presenting process control status information via graphical displays. The Final Office Action provides no basis for its assertions regarding its stated basis for motivation to modify AAPA *to render the claimed invention.* Please also consider Applicant's comments in section 4 below addressing the Final Office Action's comments at **section 22.**

3. The Final Office Action improperly disregards the "industrial process" element recited in a *non-preamble* portion of claim 1. The Final Office Action, at **section 21**, asserts that the "industrial process" can be disregarded because it is presented in the preamble. However, claim 1 recites "industrial process" within the "set of control blocks" element. The term "industrial process" cannot be ignored at least with regard to claim 1.

4. Continuing Applicant's argument that the Final Office Action does not provide a *prima facie* case of obviousness, regarding **section 22** of the Final Office Action, Applicant agrees that the teachings of the prior art references can be considered for what they teach as a whole. However, Applicant does not agree that the teachings of the cited references, when taken as a whole, teach/suggest modifying AAPA to render the claimed invention. In particular, Applicant traverses the Final Office Action's assertion that Mann, which does not even disclose a linear program providing setpoints running on a control processor, suggests modifying the prior art such that the recited embedded control task

(comprising such a linear program) is executed at a lower priority than a set of control blocks on the control processor. The Final Office Action has not addressed this aspect of Applicant's previous traversal of the rejection of the independent claims.

5. Applicant specifically traverses the rejection of claims 4 (in **section 9**) and 26 (in **section 15**) for the reasons previously stated at page 12 of the response submitted on September 20, 2005.

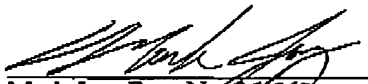
6. The Final Office Action has still not identified the recited elements of claims 8-12 and 20-24. Notwithstanding Applicant's specific request, **sections 16 and 17** of the Final Office Action continue to reject claims 8-12 and 20-24 without identifying the recited elements in the prior art reference. Applicant specifically requests reconsideration of at least the rejection of claims 8, 9, 11, 12, 20, 21, 23 and 24 in view of Applicant's previous remarks at page 13 of the September 20, 2005 response.

Conclusion

The Final Office Action has not set forth a *prima facie* case of obviousness for the rejection of the claims. Applicant submits that the prior art neither discloses nor suggests modifying AAPA to render the claimed multi-level control task execution scheme wherein an embedded multi-variable linear program, that provides setpoints for an industrial process, executes on a control processor at a lower execution priority level than a set of control blocks.

For this and other reasons submitted herein above, expedited review is requested to remedy clear errors in the Final Office Action's rejection of the pending claims.

Respectfully submitted,



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Date: June 12, 2006

Appealed Claims Appendix

1. (Previously presented) A control processor for executing a set of control tasks defining dynamic model-based interactive control of an industrial process, the control processor comprising:

an embedded control task comprising a multivariable linear program including a set of output values corresponding to process setpoints; and

a set of control blocks including regulatory control blocks having output values that are transmitted by the control processor to field devices coupled to the industrial process, wherein the embedded control task executes at a lower execution priority than an execution priority of the set of control blocks.

2. (Original) The control processor of claim 1 wherein the set of control blocks comprise supervisory control blocks.

3. (Original) The control processor of claim 2 wherein the supervisory control blocks include a multivariable control block including computer instructions facilitating communication of data between the control processor and a workstation.

4. (Original) The control processor of claim 3 wherein the multivariable control block includes computer instructions for receiving and storing a process control model to be implemented by the embedded control task.

5. (Original) The control processor of claim 2 wherein the supervisory control blocks include at least one multivariable loop block including computer instructions for providing an input value for a regulatory control block.

6. (Currently amended) The control processor of claim 5 wherein the regulatory control block is a proportional-integral-derivative block.

7. (Original) The control processor of claim 5 wherein the regulatory control block is a ratio block.

8. (Previously presented) The control processor of claim 1 further comprising a repetition cycle parameter specifying a period for re-commencing a cycle of the embedded control task.

9. (Original) The control processor of claim 8 wherein the set of control blocks includes a supervisory control block including a sequence of instructions to determine when to re-commence a cycle of the embedded task in accordance with a value specified by the repetition cycle parameter.

10. (Original) The control processor of claim 1 further comprising a block processing cycle parameter specifying a repetition period for re-commencing a cycle of executing the set of control blocks.

11. (Original) The control processor of claim 10 further comprising a repetition cycle parameter specifying a period for re-commencing a cycle of executing the embedded control task.

12. (Original) The control processor of claim 11 wherein a period specified by the repetition cycle parameter exceeds a period specified by the block processing cycle parameter.

13. (Previously presented) A method for operating a control processor, in an industrial process control environment, to establish operating values including a set of setpoint values and a set of process control variables associated with control elements in a controlled industrial process based upon a set of input variables including process variables provided to the control processor and representing the present state of the controlled industrial process, the method comprising the steps of:

executing, by the control processor, an embedded multivariable control application including computer instructions facilitating computing a setpoint value corresponding to a process control variable; and

executing, by the control processor, a set of control blocks including regulatory control blocks for receiving and storing a set of process variables representing the present state of a controlled process, wherein the embedded multivariable control application executes at a lower execution priority than an execution priority of the set of control blocks.

14. (Original) The method of claim 13 wherein the set of control blocks comprise supervisory control blocks.

15. (Original) The method of claim 14 wherein the supervisory control blocks include a multivariable control block and further including the step of downloading data from a workstation to a database accessed by the multivariable control block.

16. (Original) The method of claim 15 further comprising the steps of receiving and storing, within the database accessed by the multivariable control block, a process control model to be implemented by the embedded multivariable control application.

17. (Original) The method of claim 14 wherein the supervisory control blocks include at least one multivariable loop block, and further comprising the step of providing an input value for a regulatory control block in accordance with execution of instructions and data associated with the at least one multivariable loop block.

18. (Previously presented) The method of claim 17 wherein the regulatory control block is a proportional-integral-derivative block.

19. (Original) The method of claim 17 wherein the regulatory control block is a ratio block.

20. (Previously presented) The method of claim 13 further comprising the step of maintaining a repetition cycle parameter specifying a period for re-commencing a cycle of the embedded multivariable control application.

21. (Original) The method of claim 20 wherein the set of control blocks includes a supervisory control block, and further comprising the step of determining, by the supervisory control block, when to re-commence a cycle of the embedded multivariable control application in accordance with a value specified by the repetition cycle parameter.

22. (Original) The method of claim 13 further comprising the step of maintaining a block processing cycle parameter specifying a repetition period for re-commencing a cycle of executing the set of control blocks.

23. (Previously presented) The method of claim 22 further comprising the step of maintaining a repetition cycle parameter specifying a period for re-commencing a cycle of executing the embedded multivariable control application.

24. (Original) The method of claim 23 wherein a period specified by the repetition cycle parameter exceeds a period specified by the block processing cycle parameter.

25. (Previously presented) An industrial process control computer having multiple operating levels including:

a background control program execution level wherein the process control computer executes an embedded multivariable process control application, the embedded control application including instructions for executing a multivariable linear program to generate a set of values corresponding to process control variable setpoints; and

a foreground control block execution level wherein the process control computer executes a set of control blocks, at a higher execution priority level than the background control program execution level, the set of control blocks including program instructions that, when executed, receive and store a set of process variable values representing the state of a controlled process.

26. (Previously presented) A multi-level multivariable industrial process control program execution framework for an industrial control processor including:

a first cyclically executed sequence of instructions, repeatedly executed according to a first configurable repetition period and at a first level of execution priority, the first cyclically executed sequence of instructions including at least a set of instructions for calculating a setpoint value for a process control variable; and

a second cyclically executed sequence of instructions, repeatedly executed according to a second repetition period and at a second level of execution priority, the second level of execution priority exceeding the first level of execution priority, and thus enabling the control processor to temporarily suspend execution of the first cyclically executed sequence of instructions in order to execute the second cyclically executed sequence of instructions.